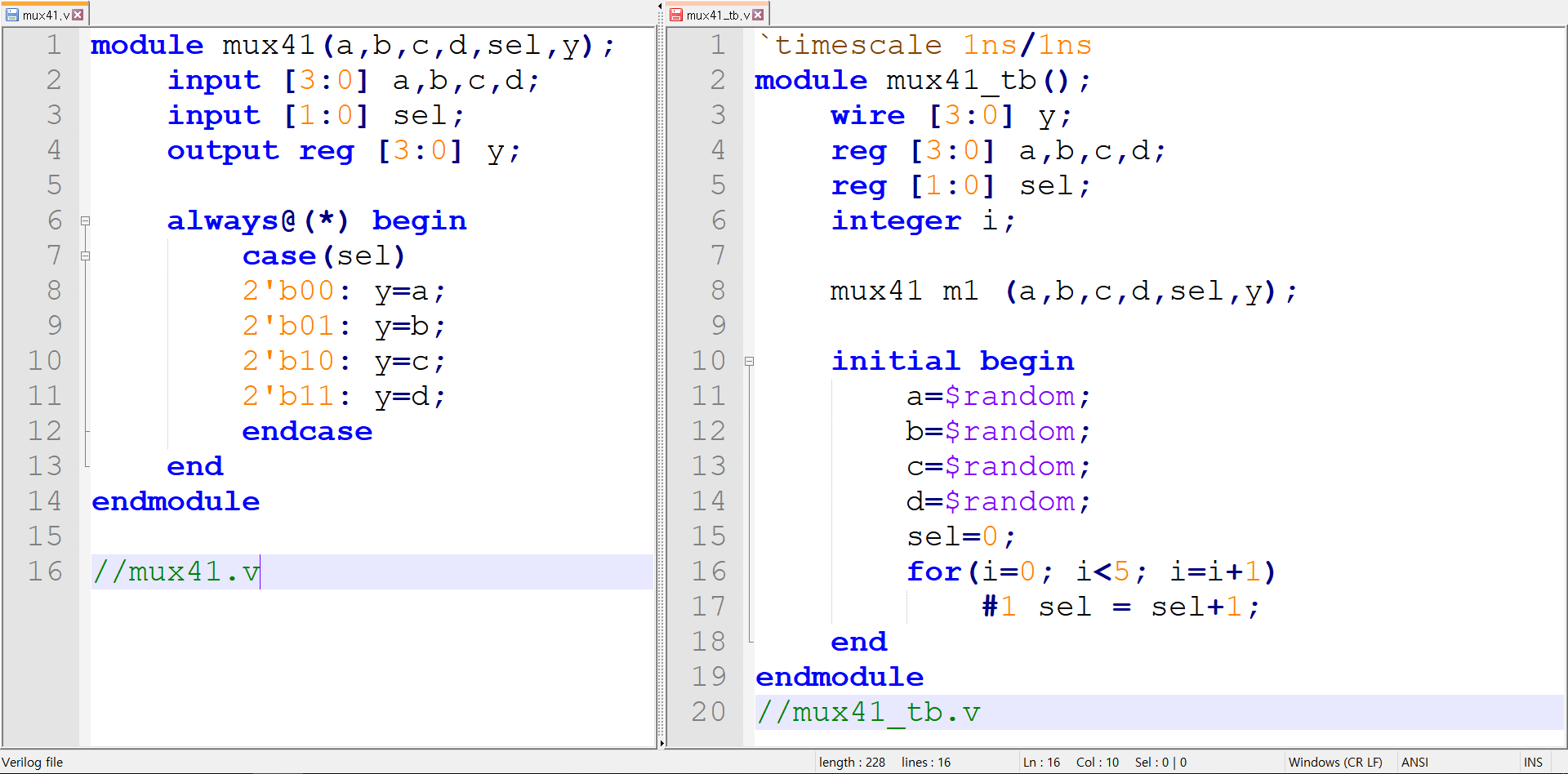
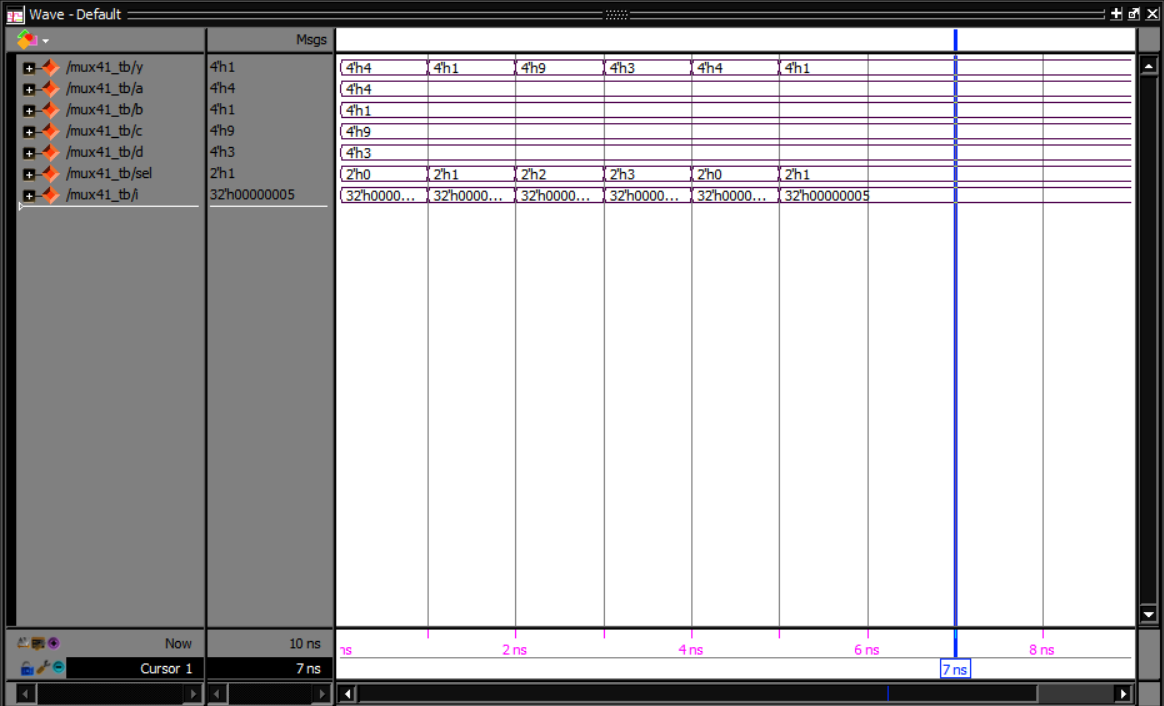
**HW2 Design a 4:1 mux**

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I make 4:1 mux using case and set input and output 4bits [3:0] , sel 2bits [1:0]

In testbench I initialized reg a,b,c,d randomly by using $random and use for to change sel value I add #1 at line 17 because in initial they didn`t show the changes of sel values